Tanta University **Faculty of Engineering** **Computer and Control Dep.** **Second Year**	**Second Term – Final Exam** **Subject: Computer Architecture** **Allowed Time: 3 Hours** **Date: 2/6/2013**

Attempt all questions and assume any missing data

Question 1: [Computer Arithmetic] — 30 Marks

1. Design 8-bit carry-lookahead adder then find the logic gate delay of S_3, S_7, C_3, C_4, C_7, and C_8.
   6 Marks

2. Use 64-bit IEEE standard for floating point numbers to represent the following numbers in binary:
   a. $(+\ 100.25)_{10}$
   b. $(-\ 22.20)_{10}$
   c. ∞

   9 Marks

3. Multiplying 11011001× 10101111 using:
   a. Booth Algorithm
   b. Bit pairing recording of multipliers
   c. Carry-save addition of summands

   9 Marks

4. Proof that the non-restoring and restoring divisions algorithms are equivalent then suggest hardware circuit for 8-bit binary division and explain its operation.
   6 Marks

Question 2: [Input/Output Organization] — 30 Marks

1. Design distributed bus arbiter scheme and explain its operation.
   6 Marks

2. What is the difference between a subroutine and an interrupt service routine?
   6 Marks

3. Design a centralized bus arbitration system that applies daisy chain between 4 I/O devices assuming that all control devices are active high. Then draw the time sequence of signals that transfer the bus mastership to device number 3.
   9 Marks

4. Design an interface circuit between the processor and a printer assuming that the computer has 32-bit address bus, 16-bit data bus, status flag bit is transferred over line D15 of the data bus, and address line A31 is used as control signal, then design the logic circuit that can generate the status flag bit properly.

9 Marks

Question 3: [Basic Processing Unit] 30 Marks

1. State the function of the input control signals of the *Control Step Counter* in the processor hardwired control unit.

4 Marks

2. Write the fetching control sequence in single-bus processor and three-bus processor.

4 Marks

3. In the single-bus processor, explain the function of the following Items:
   a. Register Z
   b. MUX
   c. PC
   d. IR

6 Marks

4. Assume that a processor has single-bus organization for its data path and run the following instruction set: Add (R1), R2 ; Move (R1), R2 ; Add R1, (R2) ; Move R1, (R2) ; Branch >0 L1 ; Increment R1 ; Move R1, R2. Use the Hardwired control scheme to design the following control signals: PC_{out}, MDR_{out}, IR_{in}.

16 Marks

Best Wishes

Dr. Tarek El.Ahmady El.Tobely